What is claimed is:

1. An HF power device in an HF transistor, comprising:

a semiconductor layer as a first conductive type;

a field area formed in a trench structure on one side of the semiconductor layer;

gate electrode formed on a given surface of the semiconductor layer;

a channel layer as a second conductive type laterally diffused from the field area to a width containing both sides of the gate electrode, and formed on the surface of the semiconductor layer;

a source area as the second conductive type formed within the channel layer between one side of the gate electrode and the field area;

a drain area as the second conductive type formed on the surface of the semiconductor layer with a given interval from another side of the gate electrode;

a sinker as the first conductive type provided as a column shape of a trench structure for dividing into two source areas by a piercing through the source area, and connected to the semiconductor layer;

an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode;

first metal electrode contacted with the source area divided into two source areas and electrically connected to the semiconductor layer through the sinker; and

second metal electrode coupled with the drain area.

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2. The device of claim 1, wherein said sinker is provided as the trench structure doped with impurity of the first conductive type on the neighborhood thereof, said trench structure having a burying of polysilicon film based on the first conductive type thereinto.

3. The device of claim 2, wherein said trench structure is provided as one or a plural number of trenches.

4. The device of claim 1, wherein said field area is any one among an oxide film grown in the trench, an oxide film gained by performing a covering on the trench and then by executing a burying thereinto through a use of a chemical mechanical polishing, and a thermal oxide film gained by performing a thermal oxidation for the trench.

5. A method of manufacturing an HF power device comprising the steps of:

forming a semiconductor layer as a first conductive type on a semiconductor substrate as the first conductive

type;

etching the semiconductor layer by a given depth and forming a first trench;

doping impurity of the first conductive type on the neighborhood of the first trench and forming a first impurity layer as the first conductive type connected to the semiconductor substrate;

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burying a conduction film as the first conductive type into the first trench;

etching the semiconductor layer by a given depth and forming a second trench with a constant interval from the first trench;

forming a field oxide film buried into the second trench;

forming gate electrode on a given surface of the semiconductor layer;

forming a source area of a second conductive type on the surface of the semiconductor layer so as to be structurally self-aligned on one side of the gate electrode and be structurally pierced by the conduction film;

forming a drain area as the second conductive type on the surface of the semiconductor layer with a given interval from another side of the gate electrode;

forming an LDD area of the second conductive type on the surface of the semiconductor layer between the drain

area and the gate electrode;

forming first metal electrode having a width which reaches the source area and the gate electrode; and

forming second metal electrode electrically connected to the LDD area.

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6. The method of claim 5, wherein in the first trench forming step, said semiconductor layer is etched by a depth reaching the semiconductor substrate.

7. The method of claim 5, wherein in the first trench forming step, one or a plural number of trenches are formed by etching the semiconductor layer.

8. The method of claim 7, wherein said first impurity layer is formed on the plural number of trenches with the conductive type same as the substrate of the first conductive type, and neighboring first impurity layers are coupled with each other to form a column shape.

9. The method of claim 5, wherein the second trench forming step is performed by etching the semiconductor layer and forming one or the plural number of trenches.

10. The method of claim 5, wherein the field oxide film

is performed by growing the thermal oxide film in the inside of said second trench.

11. The method of claim 5, wherein the field oxide film forming step comprises the steps of:

covering the semiconductor layer of the first conductive type containing the second trench with an oxide film; and

forming the field oxide film buried into the second trench by executing a chemical mechanical polishing for the covering film.